

(A)

(B)

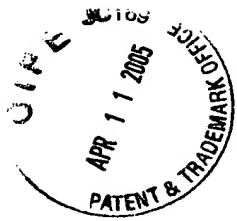


FIG. 2A

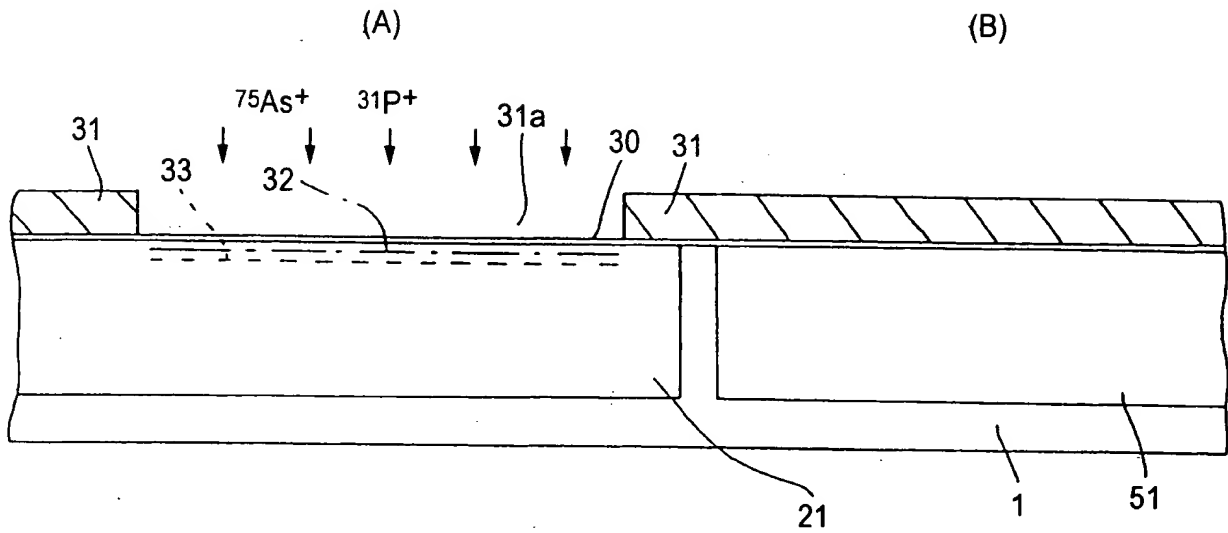
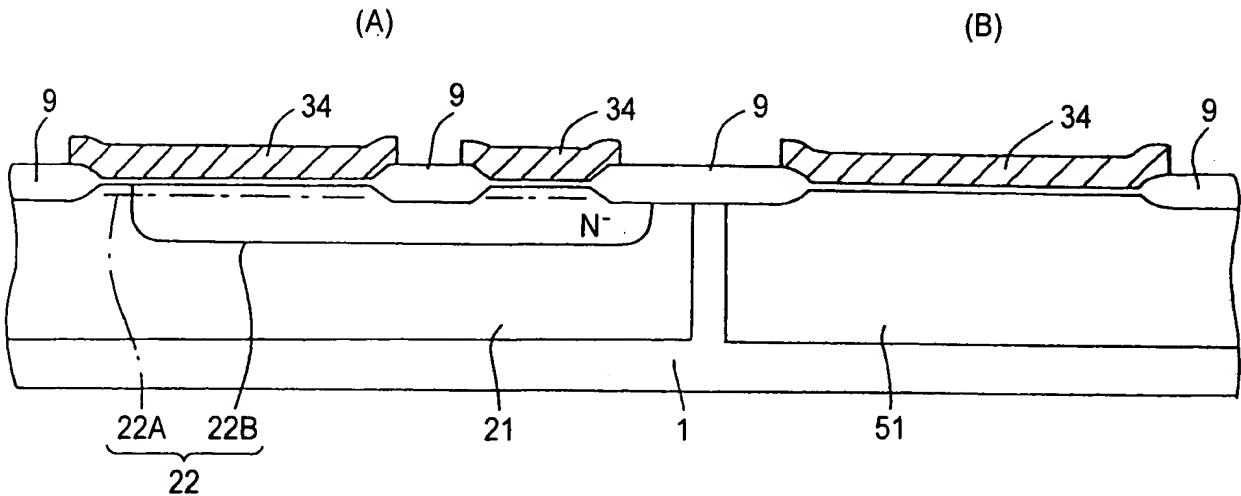


FIG. 2B



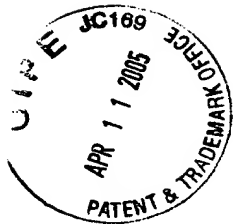


FIG. 3A

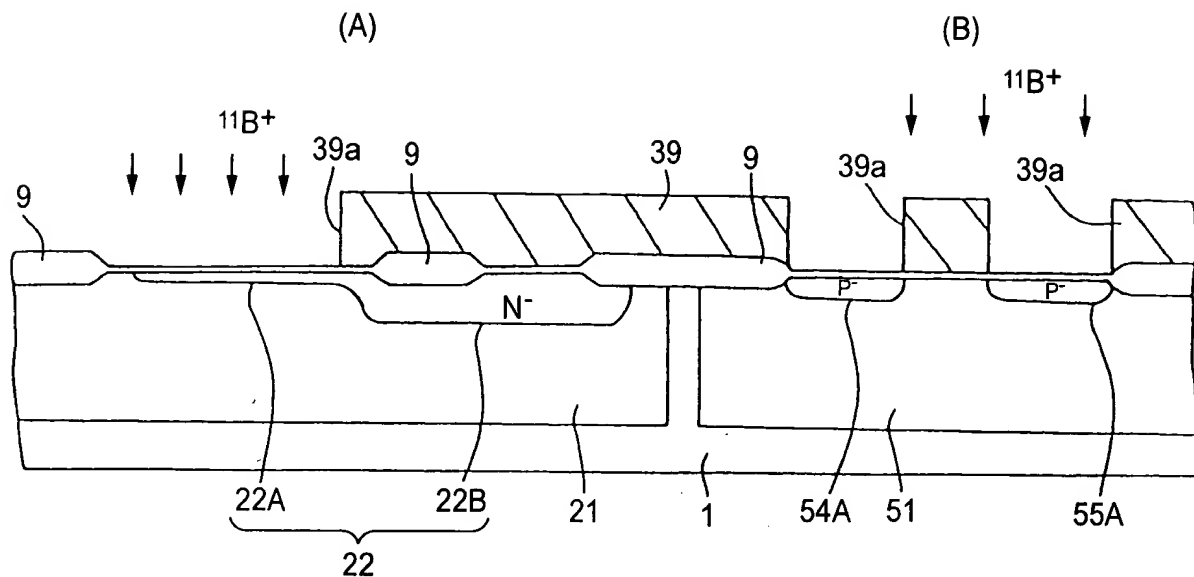
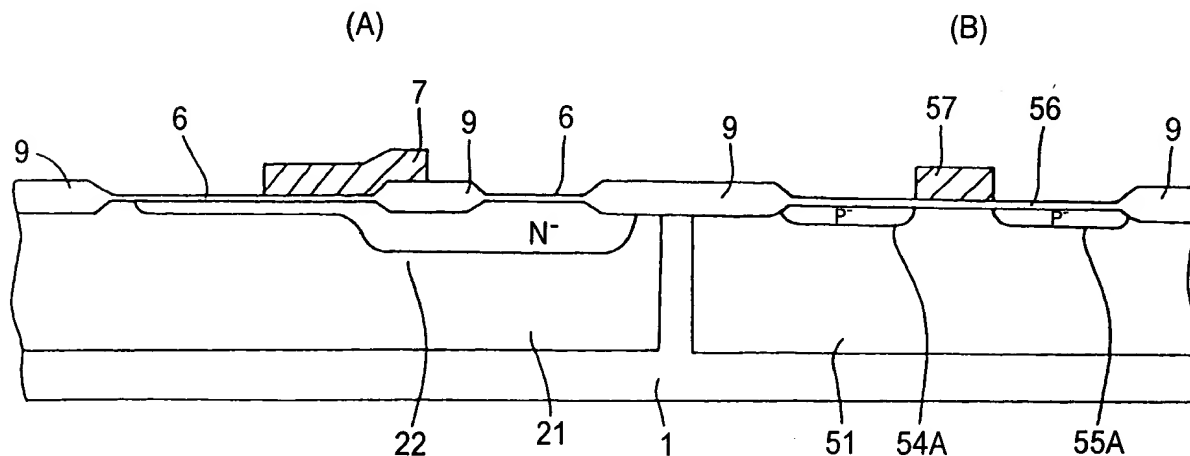


FIG. 3B



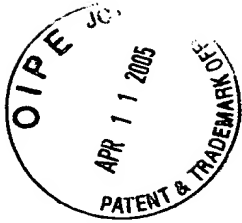


FIG. 4A

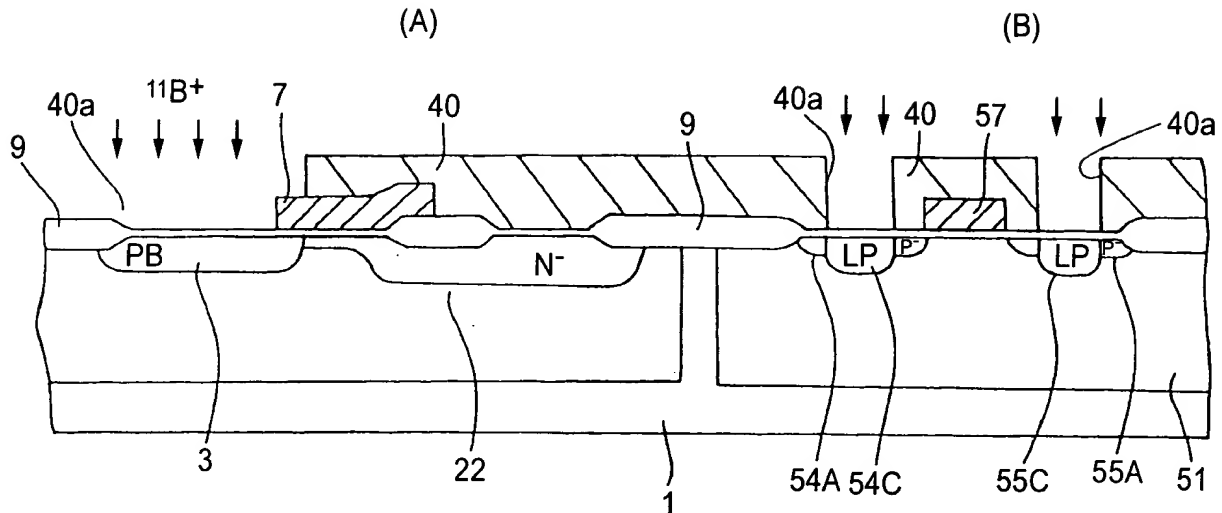
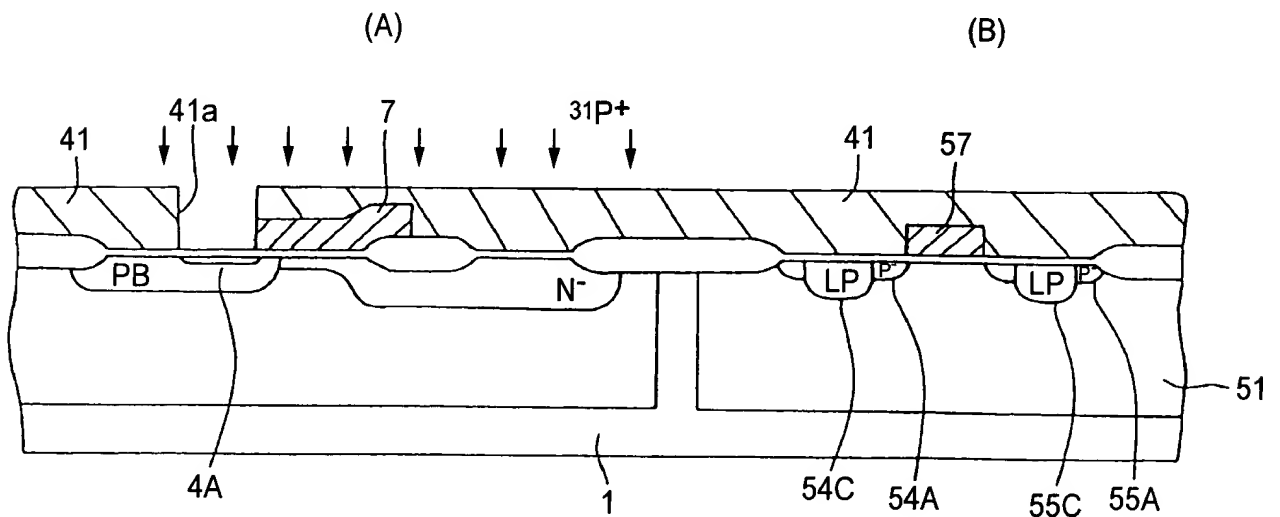


FIG. 4B



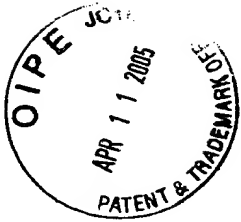


FIG. 5A

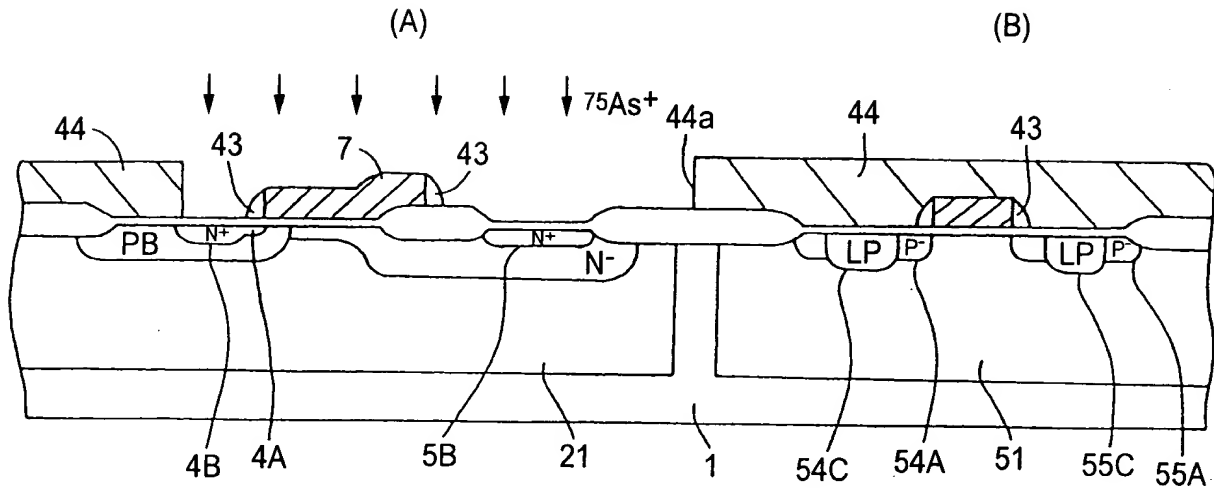
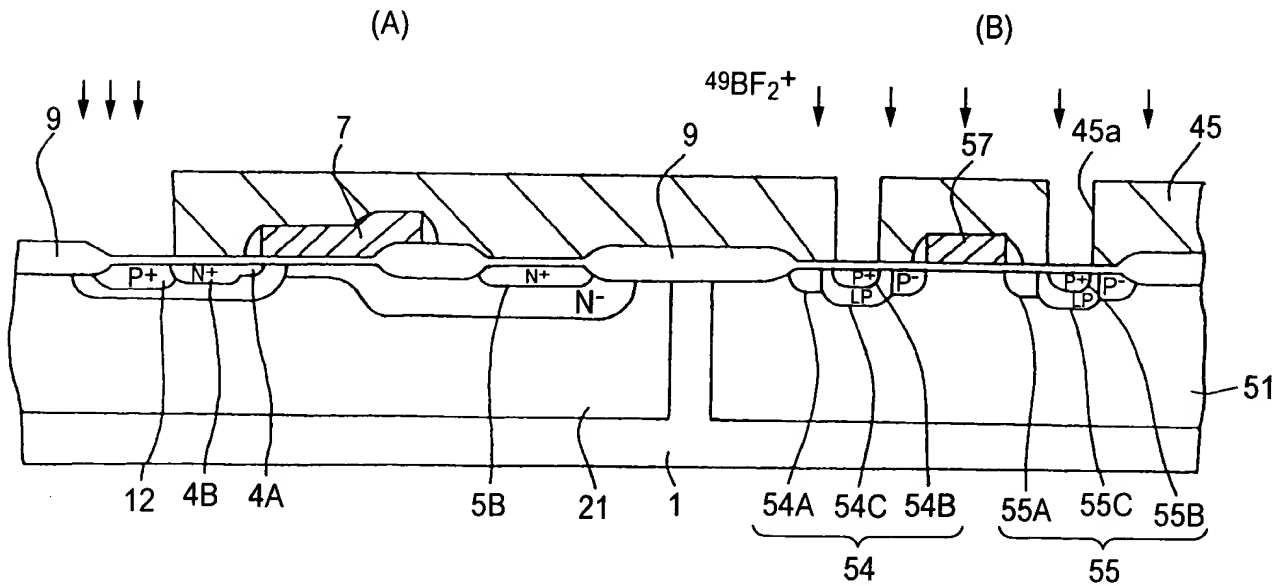


FIG. 5B



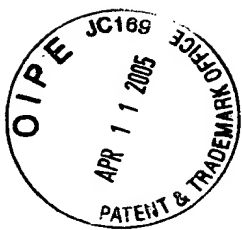
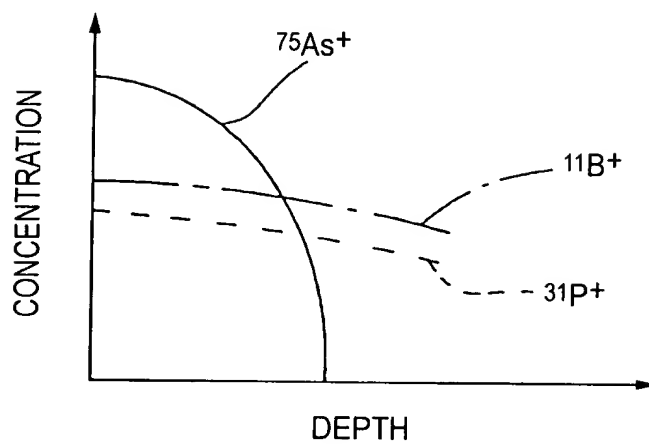


FIG. 6



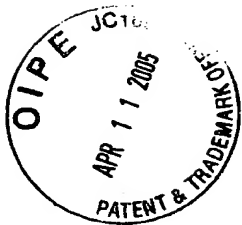
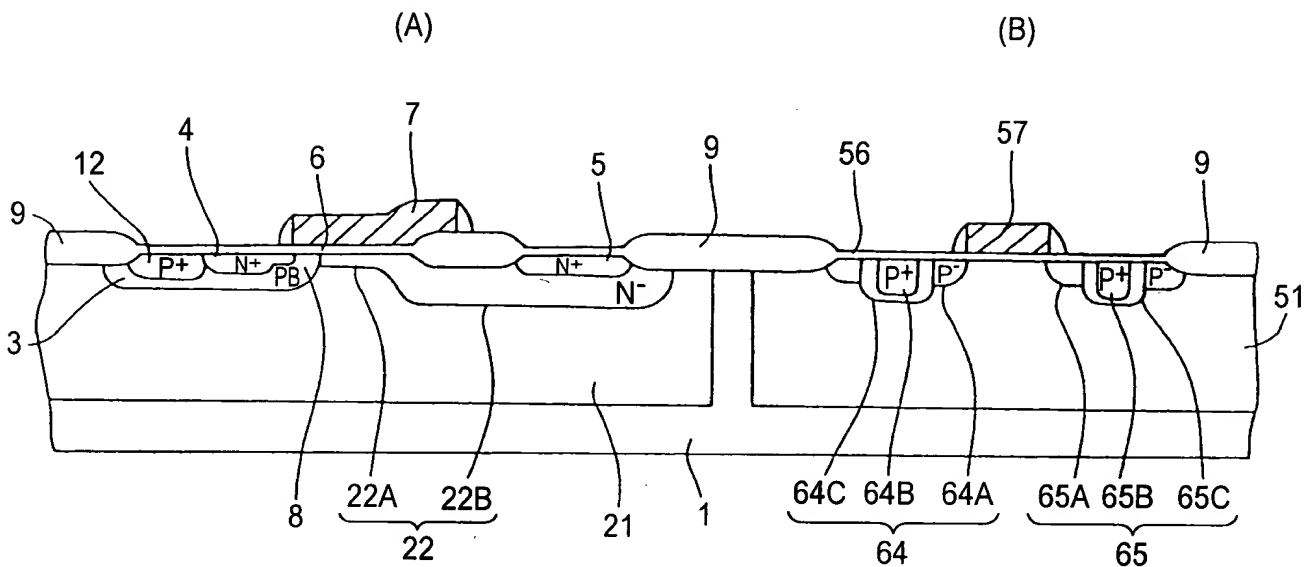


FIG. 7



[illegible]

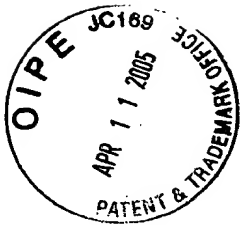
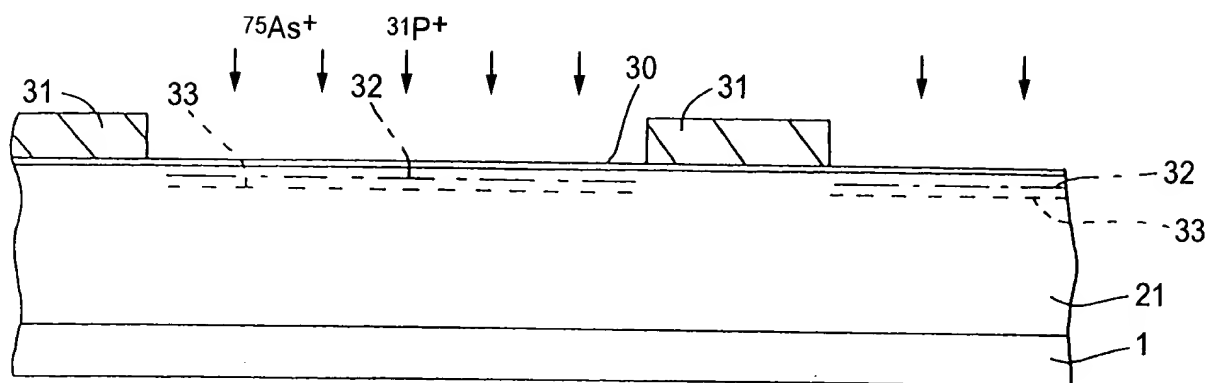


FIG. 9



This diagram shows a cross-sectional view of a semiconductor device. A gate stack is formed on a substrate, consisting of a gate dielectric layer (32) and a gate electrode layer (33). The gate stack is patterned to form a gate electrode (34). The gate electrode is covered by a gate cap layer (35) and a gate spacer layer (36). The gate spacer layer is formed on the side surfaces of the gate electrode and the gate cap layer. The gate spacer layer is patterned to form a gate spacer (37). The gate spacer is formed on the side surfaces of the gate electrode and the gate cap layer. The gate spacer is patterned to form a gate spacer (37). The gate spacer is formed on the side surfaces of the gate electrode and the gate cap layer. The gate spacer is patterned to form a gate spacer (37).

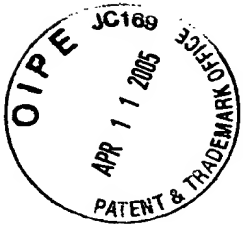
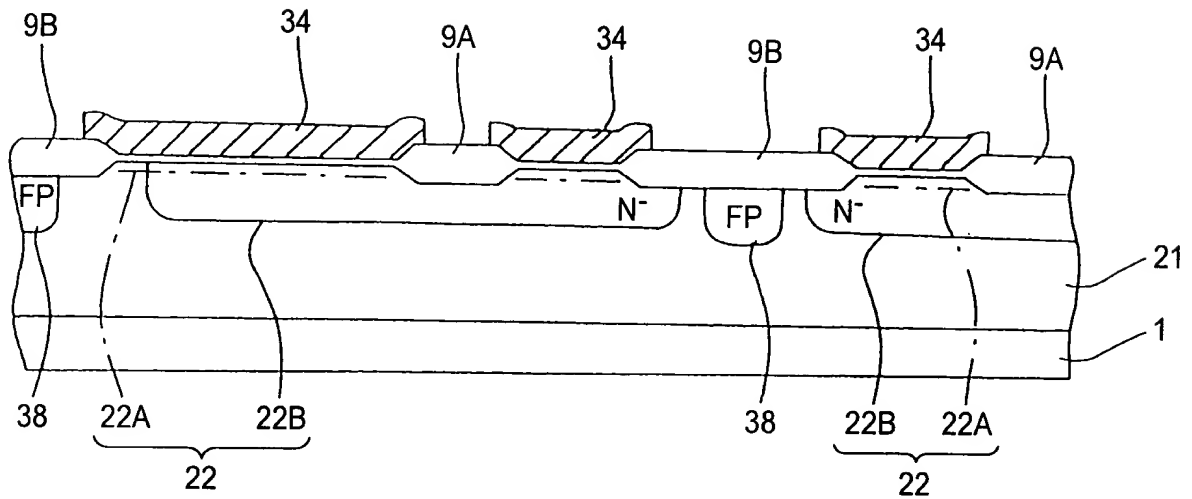


FIG. 11



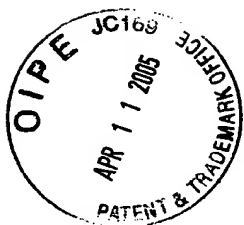
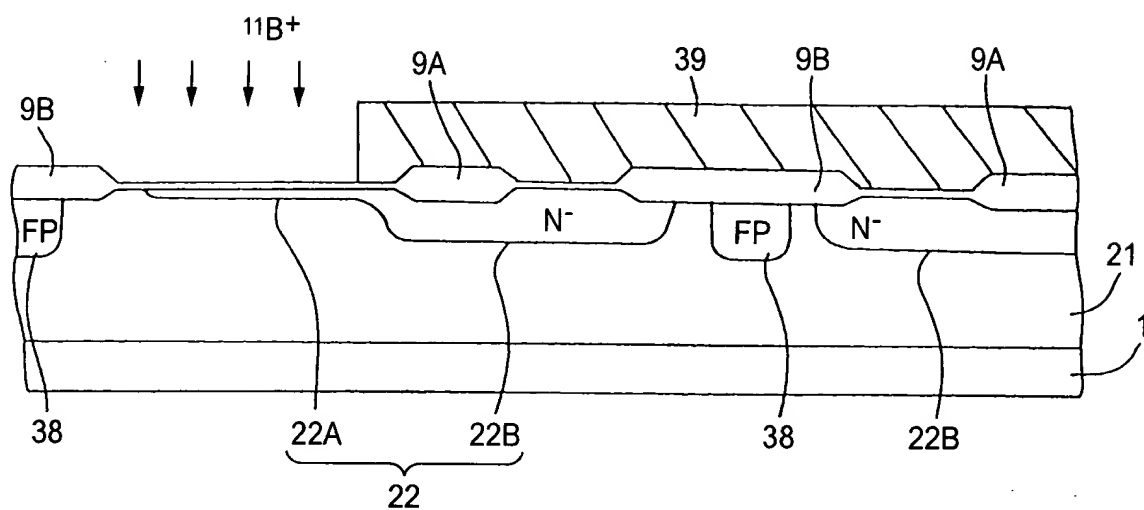


FIG. 12



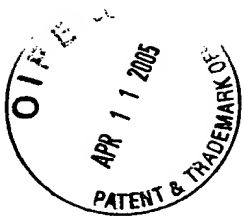
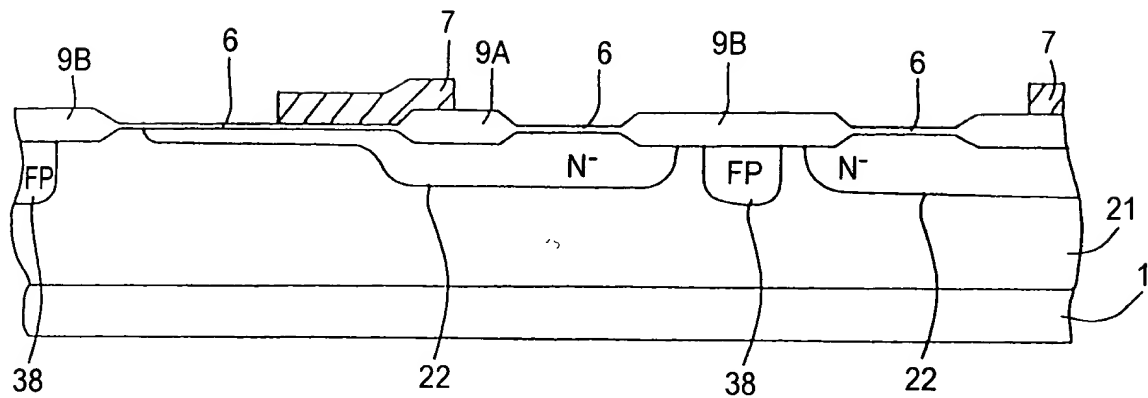


FIG. 13



Replacement Sheet

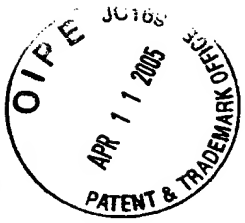
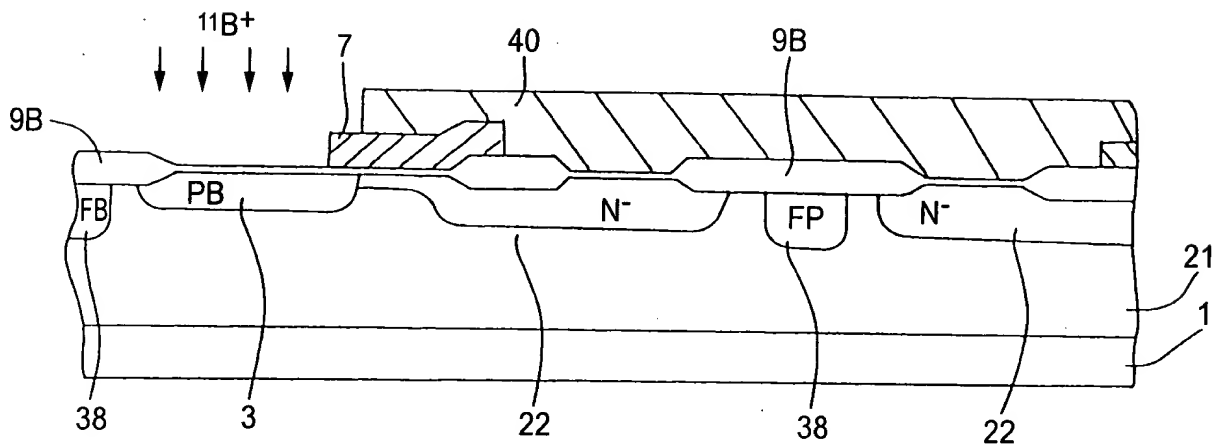


FIG. 14



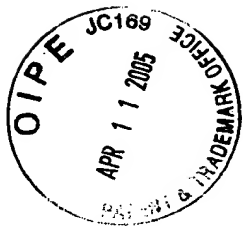
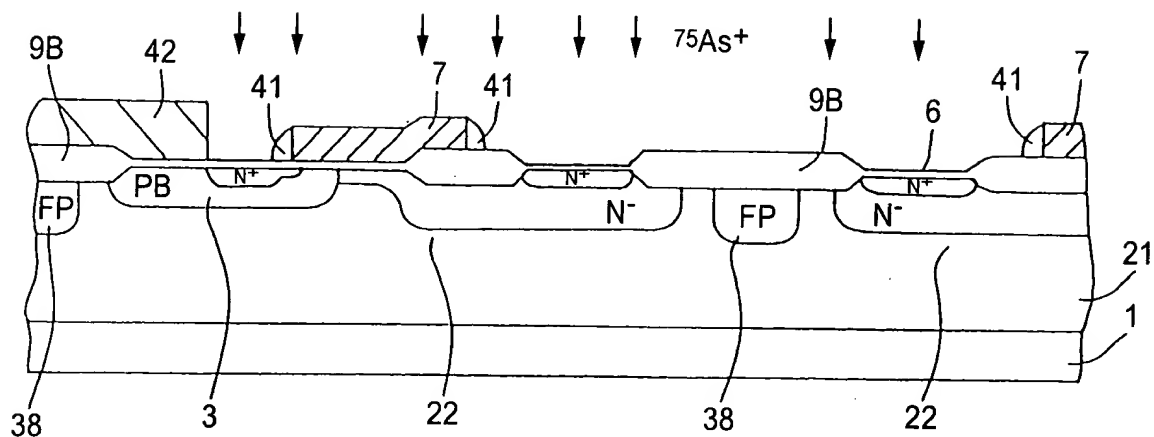


FIG. 15



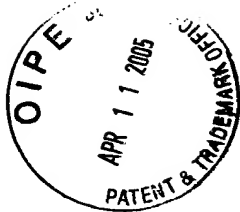
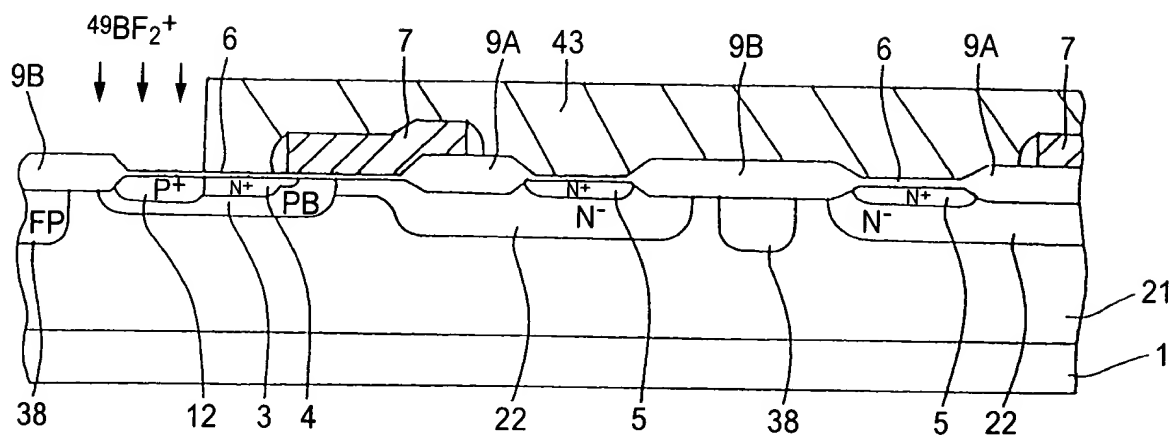


FIG. 16



This cross-sectional view shows a semiconductor device with three gate regions labeled 9A, 9B, and 9C. The device includes a substrate with layers 1, 21, and 38. Various doped regions are indicated: P+ (12), N+ (3), PB (4), and N- (5). A central region is labeled 22. The gate regions 9A, 9B, and 9C are separated by spacers 7. The device is shown in a cross-section with a central gate region 9A and two side gate regions 9B and 9C.

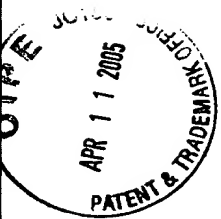
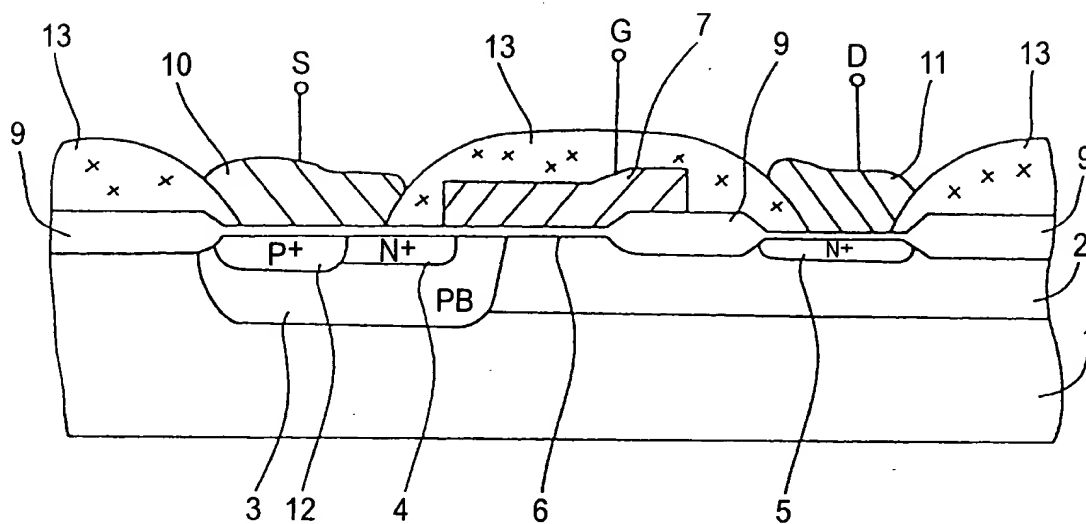


FIG. 18



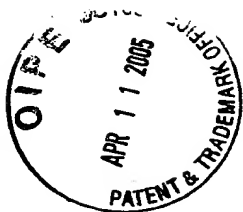


FIG. 19A

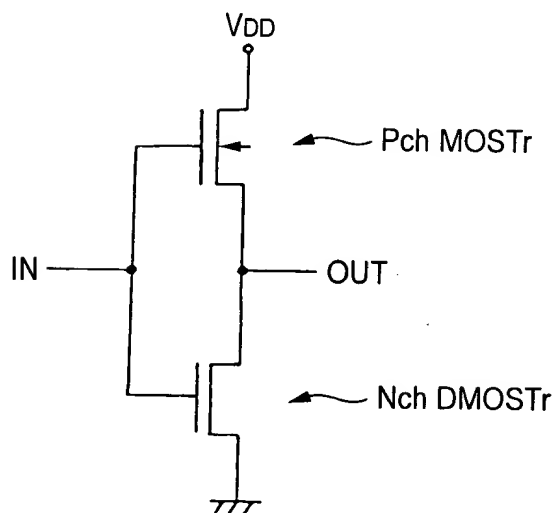
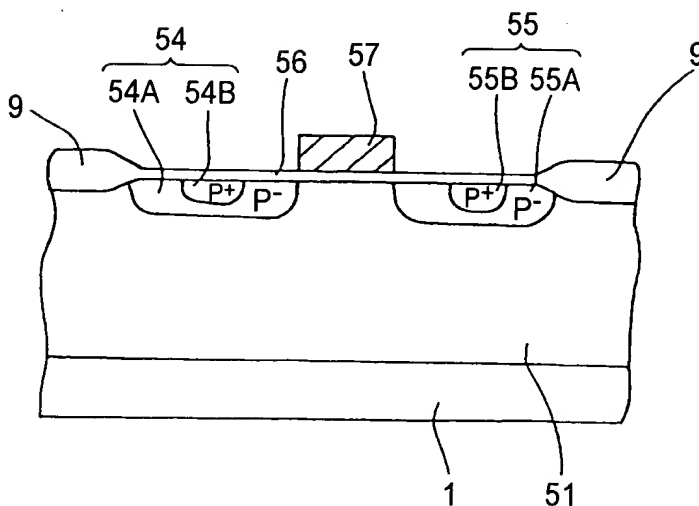


FIG. 19B



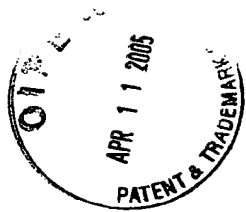
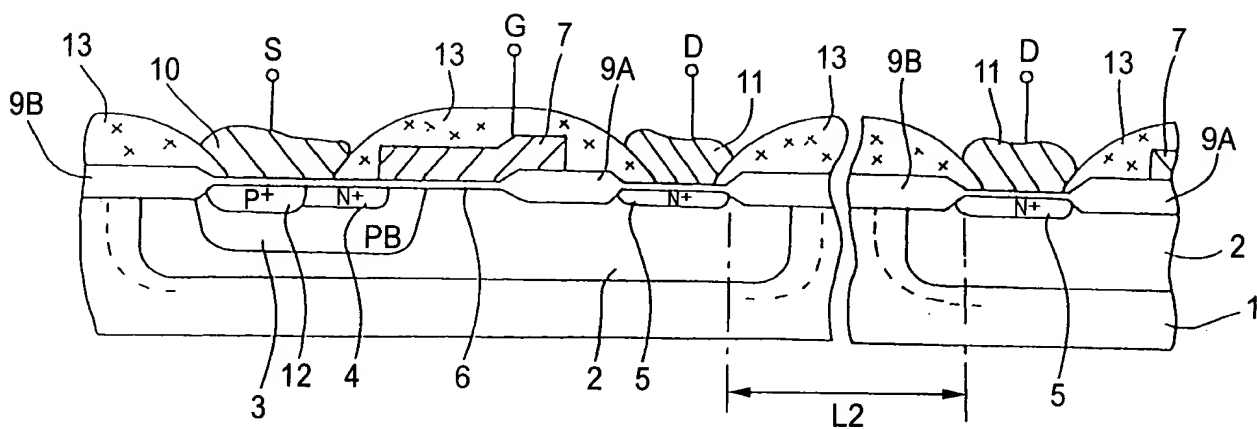


FIG. 20



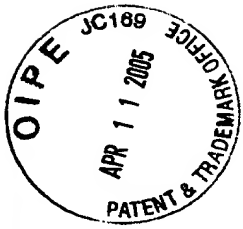


FIG. 21

N-CLAMP VOLTAGE VS. Na CONCENTRATION
STEPPED JUNCTION N-CONCENTRATION $1 \times 10^{17}/\text{cm}^3$
 $X_j = 0.2\mu\text{m}$

